In the Claims:

Please cancel claims 16-24.

There are no further amendments to pending claims 1-9, 12-15, or 25-33.

1. (previously presented) A method for forming a non-volatile memory embedded logic circuit comprising the steps of:

providing a semiconductor substrate;

forming an isolation structure on said semiconductor substrate to isolate a first device area, a second device area, and a third device area;

forming a first oxide layer on said first, second, and third device areas simultaneously, said first oxide layer providing a high voltage logic gate oxide layer in said second device area;

etching said first oxide layer in said first and third device areas to expose said substrate;

forming a second oxide layer in said first device area simultaneously with said third device area, providing a tunnel oxide layer in said first device area, a low voltage logic gate oxide layer in said third device area; and

forming a floating gate layer on top of said first oxide layer.

2. (previously presented) The method of claim 1, wherein said isolation structure is formed by a shallow trench isolation method.

3. (previously presented) The method of claim 1, wherein said isolation structure is formed by a local oxidation of silicon method.

4. (previously presented) The method of claim 1, wherein said first oxide layer is formed by thermal oxidation.

5. (previously presented) The method of claim 1, wherein said first oxide layer is formed by chemical vapor deposition.

6. (previously presented) The method of claim 1, wherein said first oxide layer is formed by atomic layer deposition.

7. (previously presented) The method of claim 1, wherein said first oxide layer is formed to approximately 250 Å thick.

8. (previously presented) The method of claim 1, wherein said second oxide layer is formed to approximately 70 Å thick.

9. (original) The method of claim 1, wherein said floating gate layer is a doped polysilicon layer.

10-11. (cancelled)

12. (previously presented) A method for forming a non-volatile memory embedded logic circuit comprising the steps of:

providing a semiconductor substrate;

forming an isolation structure on said semiconductor substrate to define a first device area and a second device area;

forming a first oxide layer on said first and second device areas simultaneously, said first oxide layer forming a high voltage logic gate oxide layer in said second device area;

etching said first oxide layer in said first device area to expose said substrate;

forming a second oxide layer in said first device area, providing a tunnel oxide layer in said first device area; and

forming a floating gate layer on top of said second oxide layers.

13. (previously presented) The method of claim 12, wherein said first oxide layer is formed by thermal oxidation.

14. (previously presented) The method of claim 12, wherein said second oxide layer is formed to approximately 70 Å thick.

15. (previously presented) The method of claim 12, wherein said floating gate layer is a doped polysilicon layer.

16-24 (cancelled)

25. (previously presented) The method of claim 1, wherein said second oxide layer is formed by thermal oxidation.

26. (previously presented) The method of claim 1, wherein said second oxide layer is formed by chemical vapor deposition.

27. (previously presented) The method of claim 1, wherein said second oxide layer is formed by atomic layer deposition.

28. (previously presented) The method of claim 12, wherein said first oxide layer is formed by chemical vapor deposition.

29. (previously presented) The method of claim 12, wherein said first oxide layer is formed by atomic layer deposition.

30. (previously presented) The method of claim 12, wherein said second oxide layer is formed by thermal oxidation.

31. (previously presented) The method of claim 12, wherein said second oxide layer is formed by chemical vapor deposition.

32. (previously presented) The method of claim 12, wherein said second oxide layer is formed by atomic layer deposition.

33. (previously presented) The method of claim 12, wherein said first oxide layer is approximately 250 Å thick.